AN2454
Application note

Universal input voltage power supply for ESBT based breaker and metering applications

Introduction

This document describes how to design a 3-phase power supply with the UC3845B PWM driver and the new STC04IE170 ESBT as main switch. It is associated with the release of the STEVAL-IPB001V1 demo board (see figure below). The design is a complete solution for the 2 W single output SMPS, which is widely used as a power supply in breaker applications. However, the design method can also be applied to an SMPS suitable for 3-phase power metering applications, as it can easily be upgraded for higher output power.

In this report particular attention has been paid to the ESBT base driving circuit, where some useful methods have been investigated to better optimize power dissipation (see *Section 6: Base driving circuit design*).

The influence of the parasitic capacitances of the transformer on the ESBT is also explained in detail (see *Section 3: Parasitic capacitances and related issues*). In addition, an active start-up circuit has been implemented on the demo board to optimize the converter efficiency, is also described (see *Section 7: Active start-up circuit*). A dedicated active component (the Darlington Q3) has been developed to support the very high voltage required (see *Figure 1*).

Finally, the most important waveforms and thermal results are given in *Section 8: Experimental results: waveforms* and *Section 9: Experimental results: efficiency and special considerations*. They demonstrate the benefits of using this solution with the start-up circuit.

Refer to AN1889 for the overall design of an auxiliary power supply using an ESBT.

STEVAL-IPB001V1 demo board

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1 Design specifications and schematic diagram

Table 1 lists the converter specifications and main parameters of the STEVAL-IPB001V1 demo board.

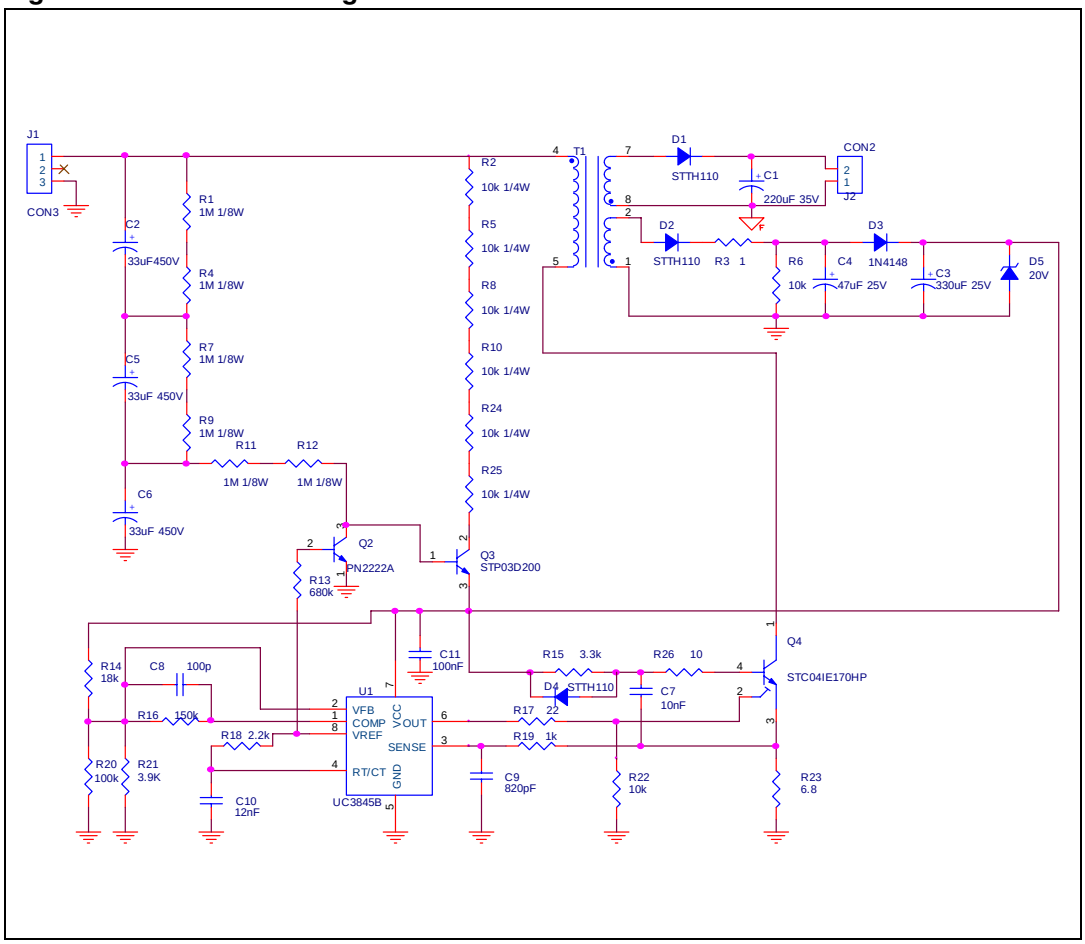
Table 1. Converter specifications and main parameters of the STEVAL-IPB001V1 demo board

Symbol	Description	Values
V_{inmin}	Rectified minimum input voltage	150
V_{inmax}	Rectified maximum input voltage	1200
V_{out}	Output voltage	24V/83mA
$P_{out\ max}$	Maximum output power	2W
$P_{out\ min}$	Minimum output power	0.2W
η	Converter efficiency	60%
F	Switching frequency	$\cong$ 50kHz
V_{fl}	Reflected flyback voltage	150V
V_{spike}	Max over voltage limited by clamping circuit	150V

A schematic diagram of the SMPS is given in *Figure 1* The most relevant components are:

- HV ESBT main switch and simple driving circuit (see *Section 6: Base driving circuit design*).
- Active start-up circuit with HV bipolar Darlington (see *Section 7: Active start-up circuit*) .
- A specially constructed transformer, with very low parasitic capacitance.

Figure 1. Schematic diagram of the SMPS



2 Flyback stage

In this section, only the main steps of the flyback stage are given. For more detailed guidelines on Discontinuous Conduction Mode (DCM) flyback converter design, refer to AN1889.

First, the transformer turn ratio, N_P/N_S, must be calculated. N_P and N_S are the respective number of primary and secondary windings. Calculation of the turn ratio is correlated to the maximum voltage rating of the transistor which is used as the primary switch. The voltage of the power switch collector, V_T, for flyback operation is given by:

Equation 1

$$V_T = V_{dcmax} + \frac{N_P}{N_S}(V_o + V_{F,\ diode}) + V_{spike} + margin$$

where

$$\frac{N_P}{N_S} \bullet (V_o + V_{F,\ diode}) = V_{fl} = \text{the flyback voltage}$$

where V_{spike} is the over voltage limited by the clamp network. It must be chosen so that the total voltage across the power switch does not exceed the maximum breakdown voltage of the power switch device (see *Equation 1*).

Once the V_{spike} voltage is fixed, the designer must choose the flyback voltage taking account of various voltage capabilities available from standard transistors. The higher the flyback voltage the higher the exploitable maximum duty cycle i.e. a higher duty cycle at fixed output power leads to a lower I_{RMS} current. This improves overall efficiency of the primary side, leading to easier design of wide input range voltage converters.

ESBTs, which have breakdown voltage capabilities as high as 2200V, offer designers a valuable tool to simplify projects from an early stage.

For the STEVAL-IPB001V1 demo board using the STC04IE170HP switch, the following parameters must be set:

- Margin = 200V.
- V_{spike} = 150V.

From *Equation 1*, the flyback vlotage (V_{fl}) gives a result of 150 V. The transformer turn ratio may then be calculated using Equation 2.

Equation 2

$$\frac{N_P}{N_S} = \frac{BV - V_{dcmax} - V_{spike} - margin}{V_o + V_{F,\ diode}} = \frac{1700 - 1200 - 150 - 200}{24 + 1} = 6$$

Once the turn ratio is calculated, the system must be stabilized to ensure that the converter operates in discontinuous mode. *Equation 3* guarantees that the energy on the primary coil will be completely transferred to the secondary coil before the next cycle occurs.

Equation 3

$$V_{dcmin}T_{onmax} = \frac{N_P}{N_S}(V_o + V_{F,\ diode})T_{reset} = V_{fl}T_{reset}$$

A safety margin of 20% is recommended to guarantee the complete demagnetization of the primary side (see *Equation 4*).

Equation 4

$$T_{onmax} - T_{reset} = 0.8T_S$$

where T_{onmax} is the maximum power-on time, T_{reset} the time needed to demagnetize the transformer inductance, and T_S the switching time.

Combining *Equation 3* and *Equation 4* , T_{onmax}, may be calculated using *Equation 5*:

Equation 5

$$T_{onmax} = \frac{V_{fl}0.8T_S}{V_{dcmin} + V_{fl}}$$

Once output power has been set to 2 W and the desired efficiency to 60%, the operating switching frequency must be chosen. To do this, a value of 50 kHz should be selected. It is then necessary to calculate the primary inductance (L_P) of the transformer. Using *Equation 6*, input power (P_{IN}) may be calculated to give an approximate value which does not account for losses due to the power switch, the input bridge and the rectified network.

Equation 6

$$P_{IN} = 1.66P_{OUT} = \frac{\frac{1}{2} \bullet L_P I_P^{\ 2}}{T_S} = \frac{\frac{1}{2}V_{onmax}^{\ 2}}{L_P T_S}$$

Using *Equation 7*, L_P may be calculated as follows:

Equation 7

$$L_P = \frac{V_{dcmin}^{\ 2}T_{onmax}^{\ 2}}{3.33T_S P_{OUT}} \approx 11mH$$

Peak current, (I_P) on the primary side may be calculated using *Equation 8*.

Equation 8

$$I_P = \frac{V_{dcmin}T_{onmax}}{L_P} \approx 110mA$$

It is also important to determine the maximum primary current, $I_{rms(primary)}$, (see *Equation 9*) and maximum secondary current, $I_{rms(secondary)}$, (see *Equation 10*) to obtain correct dimensions for the wire size of the primary windings.

Equation 9

$$I_{rms(primary)} = \frac{I_P}{\sqrt{3}}\sqrt{\frac{T_{onmax}}{T_S}} \approx 40mA$$

Equation 10

$$I_{rms(secondary)} = \frac{I_S}{\sqrt{3}}\sqrt{\frac{T_{reset}}{T_S}} \approx 240mA$$

3 Parasitic capacitances and related issues

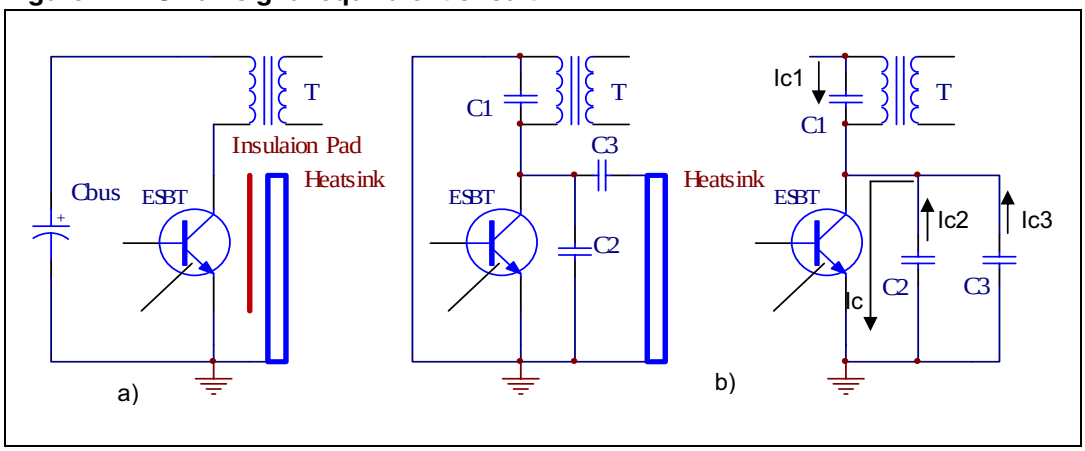
In a flyback converter stage it is important to take into account the parasitic capacitances since their influence may affect the correct operation of the converter itself. *Figure 1* shows the main schematic diagram of a flyback converter and *Figure 2* shows the small signal equivalent model.

The parasitic capacitances between the ESBT collector and ground are mainly due to three components (see *Figure 2*):

- C_1, the primary inter-winding capacitance;
- C_2, the intrinsic capacitance of the ESBT between its collector and source;
- C_3, the parasitic capacitance between the collector of the ESBT and the heat-sink.

Usually transistors are mounted on a heat-sink by interposing an insulation layer. The heat-sink has to be grounded either for safety reasons, or to minimize the RFI so that C_3 results are in the same range as C_1 and C_2. The resulting total parasitic capacitance (C) is equal to $C_1 + C_2 + C_3$. C may be large enough to produce additional and non-negligible switch-on power dissipation. Large parasitic capacitances may produce noise problems (origin ringing). Parasitic capacitance are worse at higher input voltages, like those observed in 3-phase power supply.

Figure 2. Small signal equivalent circuit



The flyback converter of the demo is operated in DCM, thus, before the end of the off-time the secondary of the transformer has discharged all energy stored in the primary inductance during the previous cycle.

Considering that the power supply is low, the transistor works without a heat sink, and consequently C_3 effects can be ignored. C_2 is related only to additional power dissipation during switch-on and does not affect system stability. C_1 has the most important affect on flyback converter design. It in turn affects:

- Parasitic transformer inter-winding capacitance.
- Layout parasitic capacitance.

Care is needed when designing the layout parastic capacitance and building the transformer.

4 Fine tuning of the application

Once the design is completed, application parameters and performance are fine tuned by bench verification.

Bench verification of the current demo board has highlighted that the chosen frequency and the high input voltage correspond with a very short conductance time. This may cause some instability or malfunctioning, even with optimized transformer parasitic elements. According to *Equation 11*, the maximum conductance time ($T_{onmax\@Vdcmax}$) at an input voltage of 1200 V is:

Equation 11

$$T_{onmaxv@Vdcmax} = \frac{L_P I_P}{V_{dcmax}} \approx 1\mu s$$

The flyback power supply tends to oscillate at maximum input voltage. The R_s resistor is in series with the ESBT as shown in *Figure 3* and has a current sensing function. The current waveform often has a large spike at its leading edge (see *Figure 4*). This is caused by the charge of the parasitic capacitance C_1. Usually, a simple RC filter is used to suppress this transient spike. The RC time constant should approximately equal the current spike duration, which is usually a few hundred nanoseconds. Values used in the demo board are:

- R_{cs} = 1 kΩ
- C_s = 820 pF.

Figure 3. Current sense circuit (a) and waveform of sense resistor (b)

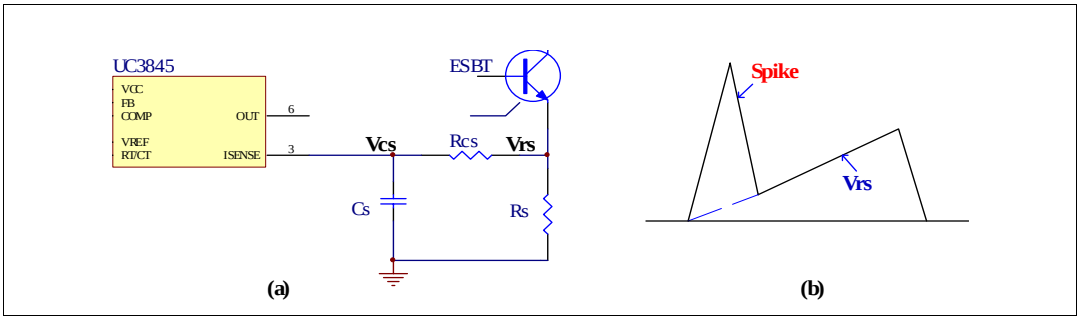
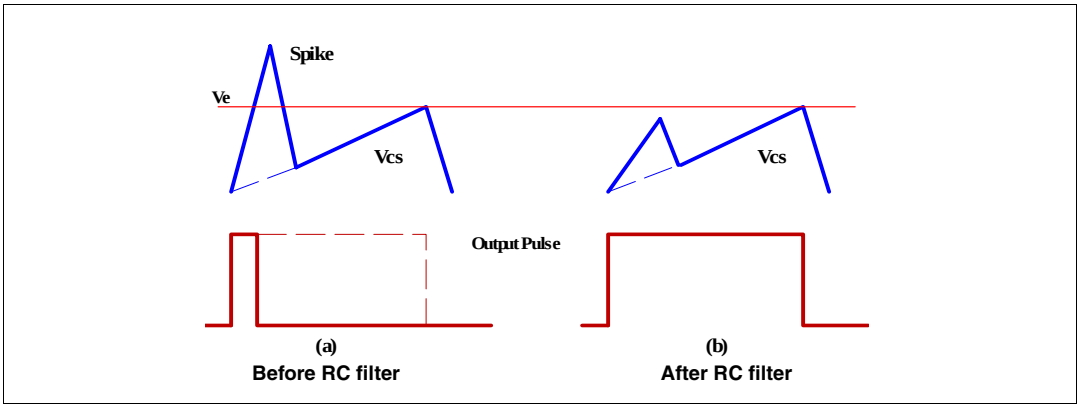


Figure 4. The normal operation waveforms of output pulse and current spike



Note that if the filter capacitance is too high, the minimum duty cycle may not be attainable and consequently there may be oscillations and instabilities. However, there may also be some instability if the filter capacitance is too small. The reason for this is as follows: energy transferred from the primary to the secondary side is small if the output pulse is prematurely terminated during the switching cycle. If this happens for several pulses, the feedback loop increases the error signal and produces a higher energy that is transferred to the secondary side. As a result, a higher output pulse is generated and again prematurely ended. Another disadvantage of a filter capacitance which is too small, is that the power supply may fail at full load and minimum input voltage. Both problems may be reduced by decreasing the parasitic capacitance between the collector and ground. This has the effect of smoothing the current spike during switch-on. In applications where switch-on occurs at very high voltages, such as single switch power supplies operating at very high input voltage, the high amount of energy stored in the parasitic capacitances leads to high peak currents and oscillations.

In the 2W SMPS, the current on the switch is very low, and even a very small peak on the leading edge during switch-on may cause the problems described above. To eliminate this problem, the parasitic capacitance must be reduced as much as possible by optimizing the layout and the transformer. When this is accomplished, the above effects can be minimized futher by additional fine tuning of the switching frequency.

Frequency reduction leads to a higher conduction time since the peak current has to be higher to develop the same output power. Of course, if frequency reduction is not followed by an increase in primary inductance, the system goes into deep discontinuous operating mode.

To stabilize the process following an increase of the primary inductance, there must be a trade off between the positive effect of a longer conduction time and the negative effect of a new reduction in the peak current.

In this demo board a switching frequency of 25-30 kHz and an inductance of 13 mH has been set.

5 Transformer design characteristics

The transformer used in this demo board has the part number SRW20EF-E13H003. Its design is not described in this application note . It is supplied by TDK and shows very low parasitic capacitance and leakage inductance.

6 Base driving circuit design

In applications such as the SMPS, where the load varies, the current of the ESBT's collector also fluctuates. To minimize losses on the power switch, a current should be provided on the base which is proportional to the collector current. It is important to avoid oversaturation of the device at low load and aim to optimize performance at full load. To achieve this a driving circuit may be used, with a current transformer, to supply the base with a current proportional to that of the collector. For additional information about ESBT base driving methods, refer to AN2131.

Figure 5 shows a simple driving circuit used for the current application. As well as being simple, it is cost effective and it minimizes power losses.

The first step in designing the base driving circuit is to set the base resistance (R_{15}). Bearing in mind that the primary peak current (I_P) of the present application is 110 mA (see *Equation 8* in *Section 2*), it is possible to calculate the base current required for the application using the dc current gain (h_{FE}) curve in *Figure 6*. For further information on h_{FE} curves, refer to datasheet STC04IE170.

Figure 5. ESBT driving circuit

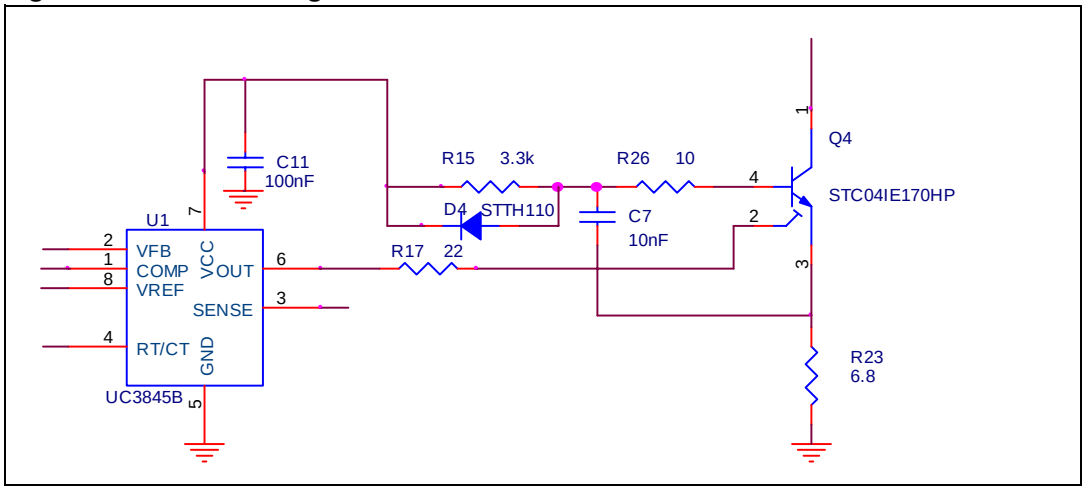
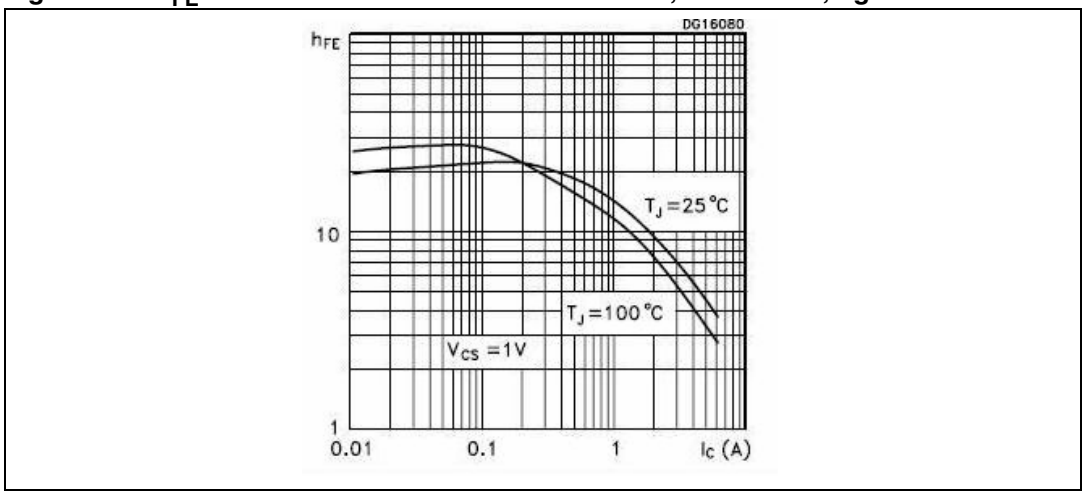


Figure 6. h_{FE} curve from datasheet STC04IE170HP, section 2.1, figure 3



At this current value (110 mA) the gain of the ESBT is about 25 (see *Figure 6*), so theoretically the current needed to drive the base should be 4.4 mA (110/25). This is true for very long conduction times. However, for the present application, a dynamic saturation phenomenon may occur due to a combination of relatively high switching frequencies (about 30 kHz) and small conduction times (1 µs at full load and maximum input voltage).

The dynamic saturation effect, which is observable in all "bipolar devices" during switch-on operations, is related to the delay of the voltage drop between collector and emitter in reaching the static value (V_{CESAT}). In general, the higher the working frequency, the worse the dynamic saturation effect is. A method which is commonly used to moderate this effect, is to inject the base quickly and heavily with minority carriers, thereby providing a very high current peak at switch-on. The resulting high base current conflicts with the need not to oversaturate the device because it impacts badly on switch-off losses. In fact, benefits obtained at switch-on may actually be a weakness at switch-off.

To summarize, a base current higher than the theoretical value of 4.4 mA has to be provided to enhance conduction performances by reducing the voltage drop just after switch-on. However, if the base current is increased arbitrarily, switch-off may be too slow and overly dissipative. A good trade off may be achieved if the dimensions of the base capacitor are small enough to provide a very high but short current peak to the base.

Note that during storage time the collector current flows through the base and gets stored in the base capacitor so that a quasi total recovery of energy is achieved.

Using *Equation 12*, the time duration of the base current spike (t_{PEAK}) may be calculated to give an approximate value:

Equation 12

$$t_{peak} = 3R_{26}C_7$$

To achieve a T_{peak} of 300 ns, and since the value of R_{26} is set to 10 Ω, then capacitor 7 (C7) may be calculated using *Equation 13* to give a value of 10 nF:

Equation 13

$$C_7 = \frac{t_{peak}}{3R_{26}} = 10nF$$

Knowing that V_{CC} is approximately 15V, R_{15} may be calculated to give a value of 3.4 kΩ:

Equation 14

$$R_{15} = \frac{15V}{4.4mA} = 3.4k\Omega$$

The closest commercial value available for R_{15} is 3.3 kΩ

7 Active start-up circuit

A non-dissipative, active start-up circuit has been implemented to optimize converter efficiency. The alternative option to use a pure resistive start-up circuit was rejected because total converter efficiency would have been extremely low due to the low output power (2 W).

To select the components of the start-up circuit, the following steps should be followed:

1. Find the minimum start-up current ($I_{UC3845B\text{-}start\text{-}up}$) required by the I_C driver. Referring to datasheet UC3845B, $I_{UC3845B\text{-}start\text{-}up}$ has a value of 0.5 mA.
2. Set the maximum start-up resistance ($R_{start\text{-}upmax}$), paying particular attention to the driver consumption (see above) and using *Equation 15* below.
3. Set the start-up capacitor according to the start-up and UVLO threshold of the UC3845B and total consumption during start-up time (i.e. the time between the points when start-up threshold and output and auxiliary steady state voltage are reached).
4. Verify the relevant start-up time and test the wake-up time.
5. Fine tune the necessary components. For example, if wake-up time is too long the start-up resistors need to be reduced. If start-up time is too long C_3 (capacitor 3) in *Figure 1* may need to be increased.

Using *Equation 15* the maximum start-up resistance ($R_{start\ -\ upmax}$) may be calculated:

Equation 15

$$R_{start-upmax} = \frac{V_{dcmin}}{I_{UC3845-start-up}} = 300k\Omega$$

The additional power dissipation (P_{Rstart}) due to the start-up circuit at maximum input voltage may then be calculated using *Equation 16*.

Equation 16

$$P_{Rstart} = \frac{1200^2}{300 \bullet 10^3} = 4.8W$$

However, when $V_{dc} = V_{dcmax} = 1200$ V, a value of 4.8 W is unacceptable since the maximum output power is 2 W.

This problem cannot be solved even if the I_C driver is replaced by the L_{6565} which uses a much lower start-up current. Referring to datasheet L_{6565}, $I_{L6565\text{-}start\text{-}up}$ has a value of 70 µA. Substituting into *Equation 17*, *Equation 18*, a value of 0.66 W for the additional power dissipation is still too high since it represents about 33% of total output power.

Equation 17

$$R_{start-upmax} = \frac{V_{dcmin}}{I_{L6565-start-up}} = 2.15M\Omega$$

Equation 18

$$P_{Rstart} = \frac{1200^2}{2.15 \bullet 10^6} = 0.66W$$

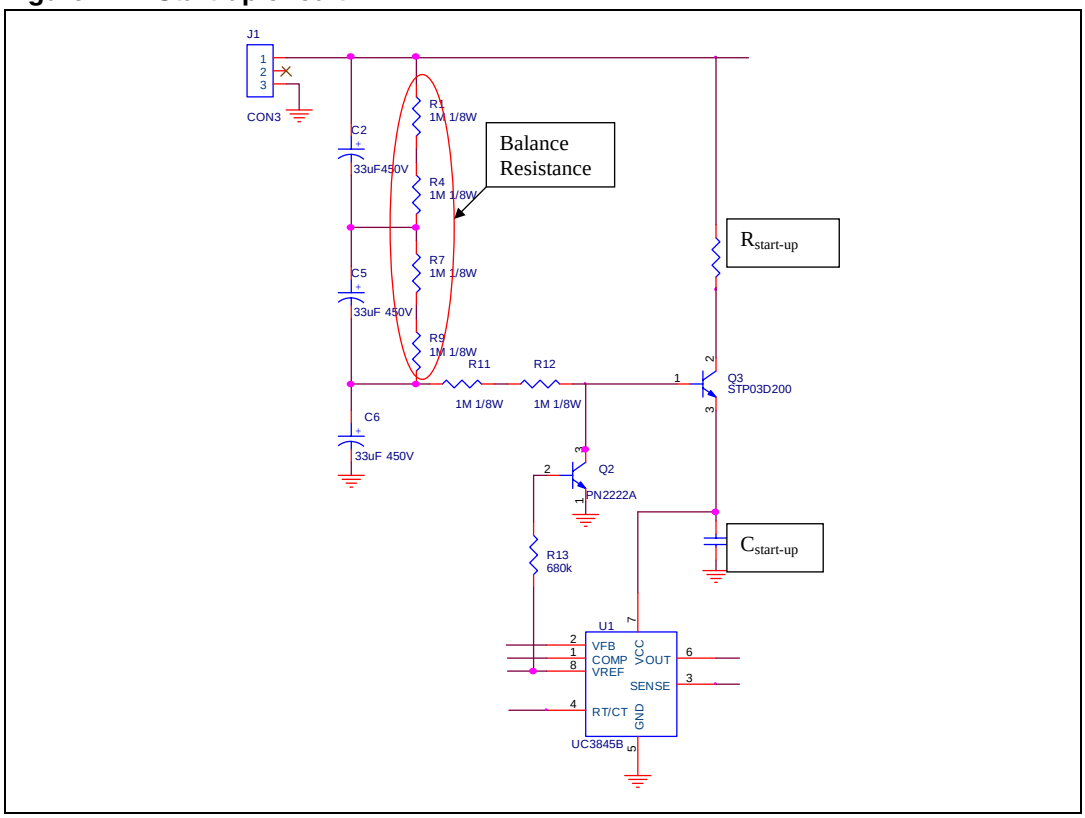
Clearly, an active start-up circuit is essential to increase converter efficiency. Moreover, it allows the use of the simplist, low cost PWH driver.

Figure 7 shows the start up circuit used in the present demo board. The start-up resistance comprises a series of 6 resistors, while $C_{start-up}$ is in parallel with C_3 and C_{11} (see *Figure 1*).

The balance resistances shown in *Figure 7*, are used to ensure the same voltage drop across each input capacitor and to supply the current to the base of the Q3 Darlington before V_{CC} reaches the device threshold. During this time V_{REF} input of UC3845B is low and Q2 is off.

When V_{CC} reaches the start-up threshold (typically 8.4 V), V_{REF} is high (5 V) and Q2 is turned on. Q3 is turned off which disconnects the start-up current path. The additional power dissipation under such normal working conditions is due to the balance resistances. They may be set at very high values.

Figure 7. Start-up circuit



As an active start-up circuit is being used, the start-up current may be over set by fixing the start-up resistance correctly. However, first the start-up capacitor must be calculated.

The start-up capacitor feeds the PWM driver of the UC3845B device until the auxiliary supply voltage rises. Using the UC3845B datasheet and assuming a start-up time of 10 ms (which should be validated on the bench), the minimum start-up time ($C_{start\text{-}upmin}$) may be calculated as follows:

Equation 19

$$C_{start-upmin} = \frac{\Delta Q}{\Delta V} = \frac{I_{UC3845quiescent} Tstart-up}{V_{start-up} - V_{UVLO}} = \frac{17mA \bullet 10ms}{8.4 - 7.6} = 212.5\mu F$$

If a wake-up time ($T_{wake\text{-}up}$) of 1 s is set, as a worst case scenario, $T_{wake\text{-}up}$ may be calcluated using *Equation 20*:

Equation 20

$$T_{wake-up} = \frac{C_{start-upmin} V_{start-up}}{I_{totstart-up}}$$

The total start-up current ($I_{totstart\text{-}up}$) needed before start-up may then be calculated using *Equation 21*:

Equation 21

$$I_{totstart-up} = \frac{C_{start-upmin} V_{start-up}}{T_{wake-up}} = \frac{220\mu F \bullet 9V}{1s} = 1.98mA$$

Hence, start-up resistance (R_{start}) may be calculated using *Equation 22*:

Equation 22

$$R_{start} = \frac{V_{dcmin}}{I_{totstart-up}} = \frac{150V}{2mA} = 75K\Omega$$

The balance resistance values also need to be set. These resistances are needed to provide current to the base of the Darlington.

Given that:

$$\frac{I_{totstart-up}}{h_{FEDarlington}} = \frac{2mA}{500} = 4\mu A$$

and assuming the worst Darlington gain is 500, total balance resistance ($R_{totbalance}$) may be calculated using *Equation 23*:

Equation 23

$$R_{totbalance} = \frac{150V}{4\mu A} = 37.5M\Omega$$

As the maximum voltage applied to the resistors is 1250 V and as approximately no more than 250 V should be applied to each individual resistor, then taking a small margin of error into account, six resistors of 5.6 mΩ each can be selected.

Therefore total additional losses ($P_{Rbalance}$) may be calculated using *Equation 24*:

Equation 24

$$P_{Rbalance} = \frac{1250V^2}{33.6M\Omega} = 0.046W$$

Total additional losses can be seen to have no negative impact on total efficiency.

8 Experimental results: waveforms

Figure 10 to *Figure 20* below show the main waveforms under steady state conditions at full load. Of particular importance is the behavior of the base current, where an initial high peak pulse is needed to minimize the effect of the dynamic saturation voltage.

Figure 8. Minimum input voltage: storage highlighted

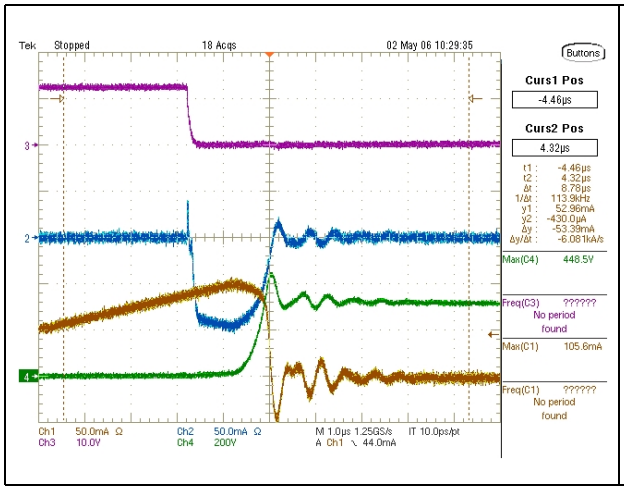


Figure 9. Minimum input voltage: switch-on highlighted

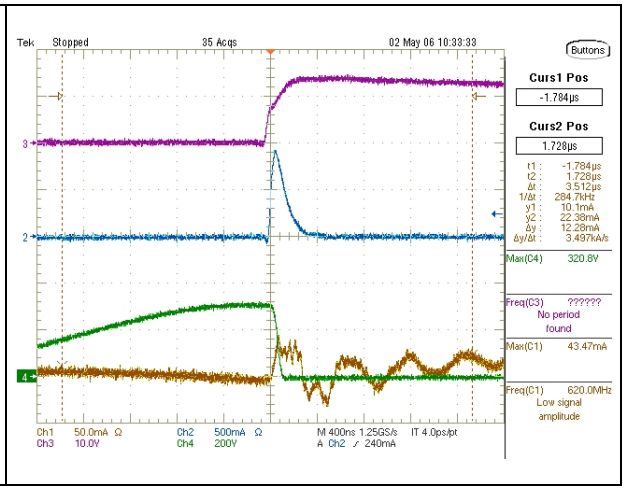


Figure 10. Minimum input voltage 1

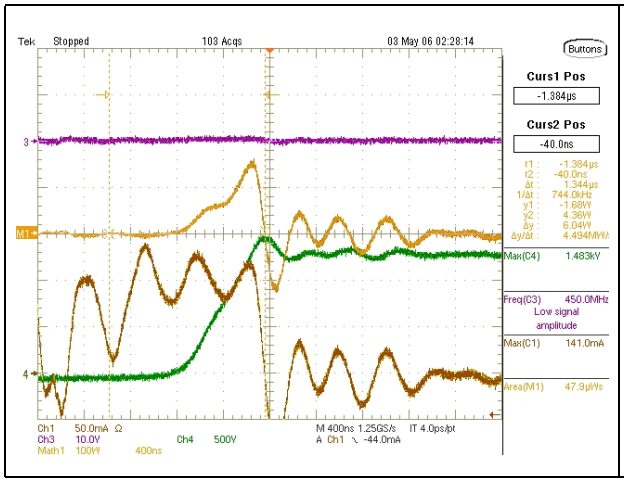


Figure 11. Minimum input voltage 2

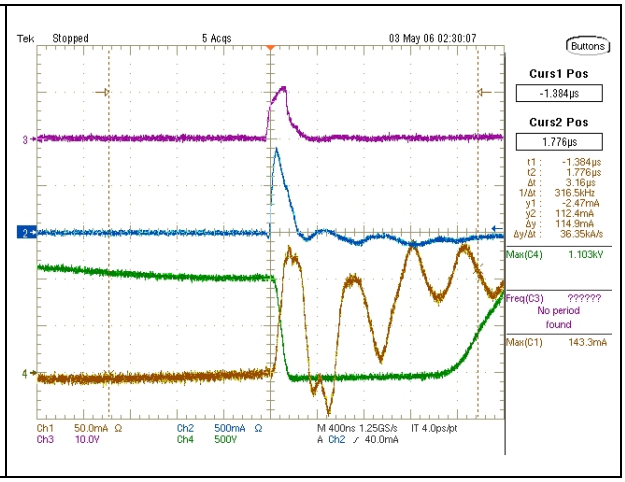


Figure 12. Minimum input voltage: switch-off highlighted

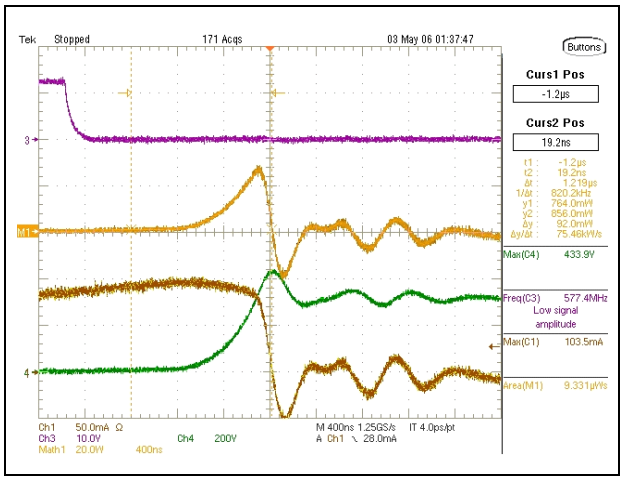


Figure 13. 560V input voltage 1

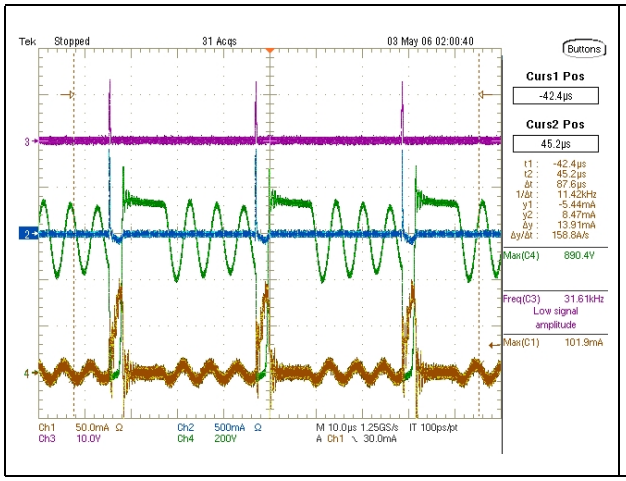


Figure 14. 560V input voltage 2

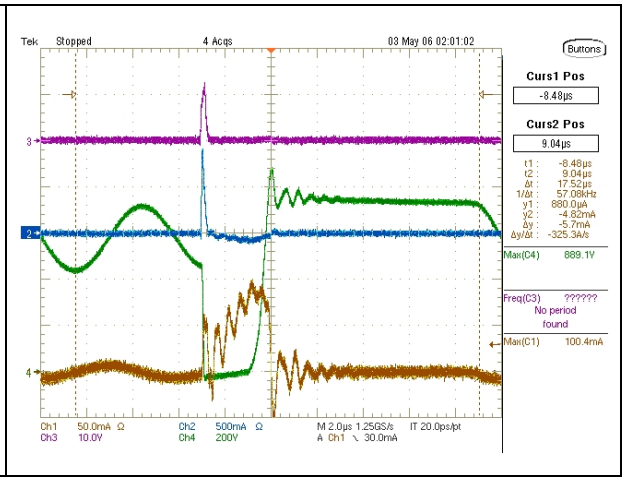


Figure 15. 560V input voltage: switch-on highlighted

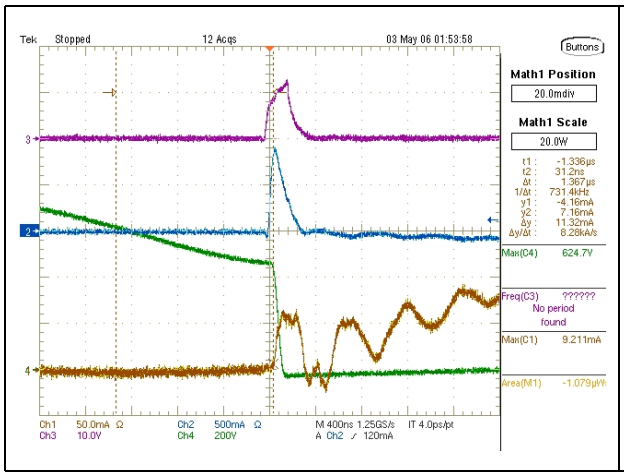


Figure 16. 560V input voltage: switch-off highlighted

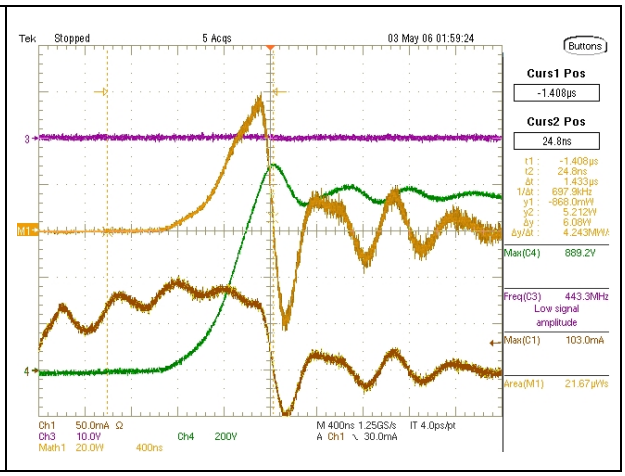


Figure 17. 1050V input voltage 1

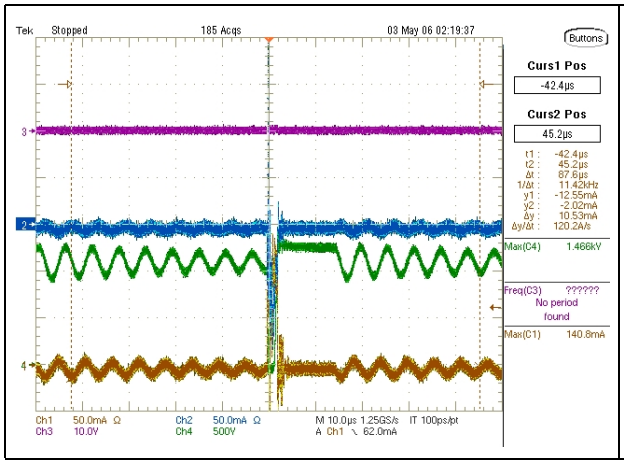


Figure 18. 1050V input voltage 2

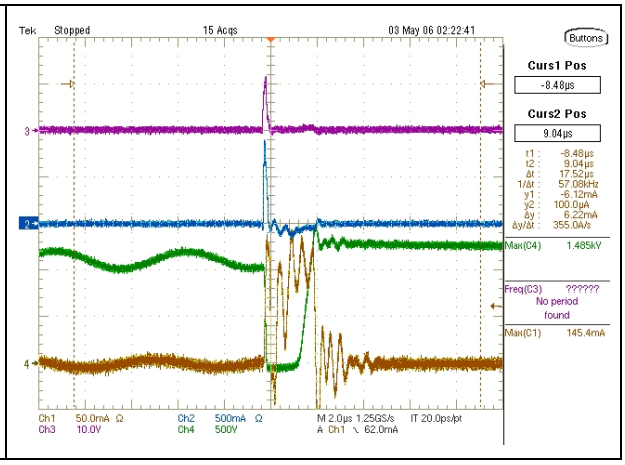


Figure 19. 1050V input voltage: switch-off highlighted

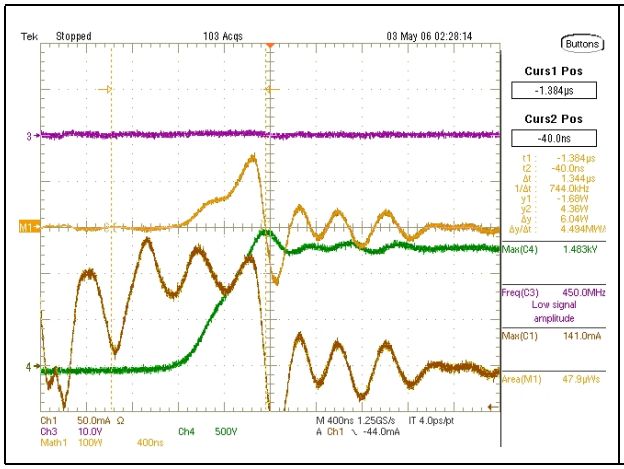
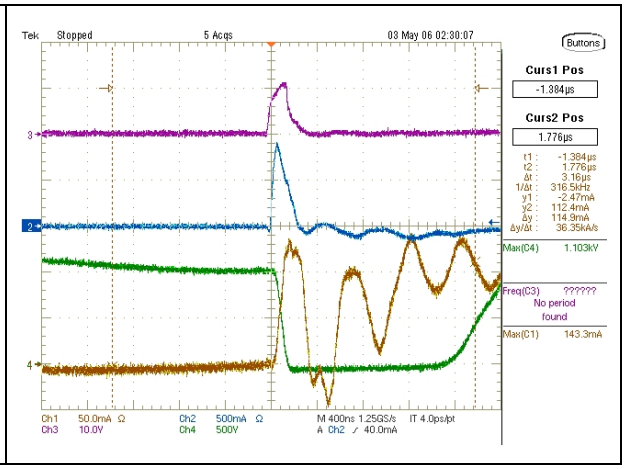


Figure 20. 1050V input voltage: switch-on highlighted



9 Experimental results: efficiency and special considerations

Table 2 summarizes the experimental results for case temperature (T_c), total losses (P_{tot}), and efficiency. All information refers to maximum load. Relatively high efficiency was achieved (60%) even at the highest input voltage of 760 V. Also, the case temperature is quite low (47°C) even with low power dissipation (0.44 W).

Table 2. Experimental results

VinAC (V)	Tc (°C)	Ptot (W)	Efficiency
110 (V)	33	0.16	80%
400 (V)	37	0.24	73%
760 (V)	47	0.44	60%

To achieve the thermal performances shown in *Table 2*, a special feature of the bipolar Darlington has been used: when the input voltage continues to rise, the switching losses increase at fixed frequency operation. Consequently, the storage time of the ESBT is quite long (about 1.5µs), resulting in a minimum conduction time higher than 1.5µs. Thus, the system is forced to work in burst mode when input voltage increases.

In *Figure 21* and *Figure 22*, the peak value of I_C is constant and no burst mode is present.

Figure 21. 110 Vac envelope

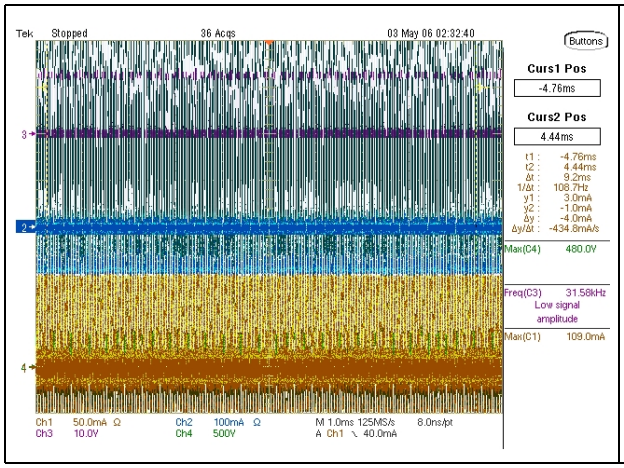
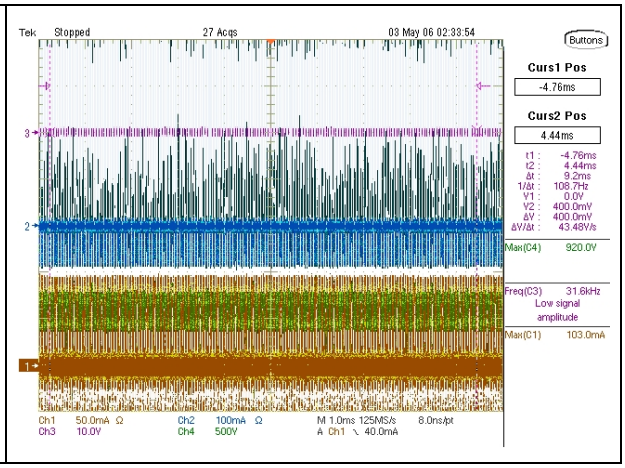


Figure 22. 220 Vac envelope



A constant value for I_C holds true for input voltages up to 420Vac. Burst mode starts to appear at 420Vac (*Figure 23*), becoming more and more obvious at higher input voltages (*Figure 24* and *Figure 25*).

Burst mode is a "natural" phenomenon which arises due to the storage time. It allows the total power dissipation of the device to remain low regardless of the very high voltages being sustained.

Thus, without adding any additional functions and by using the simplest PWM driver available on the market, the switching frequency may be decreased by reducing the number of switching cycles.

Finally, when burst mode frequency is very high the switching frequency becomes 15 kHz. Consequently, the switching frequency has been halved due to the storage time which acts as a delay on the switch-off of the ESBT (see *Figure 26*).

Figure 23. 420 Vac envelope

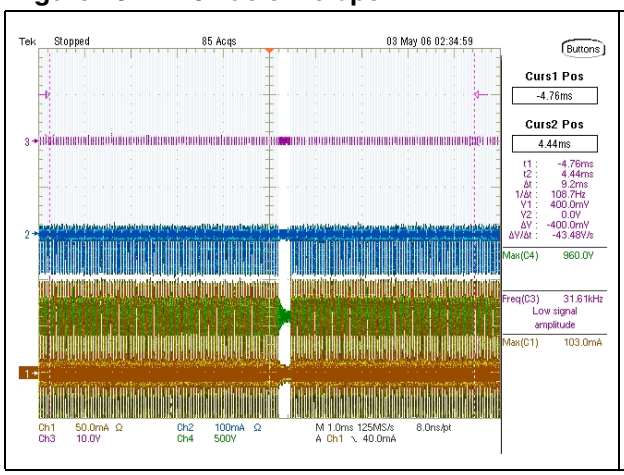


Figure 24. 480 Vac envelope

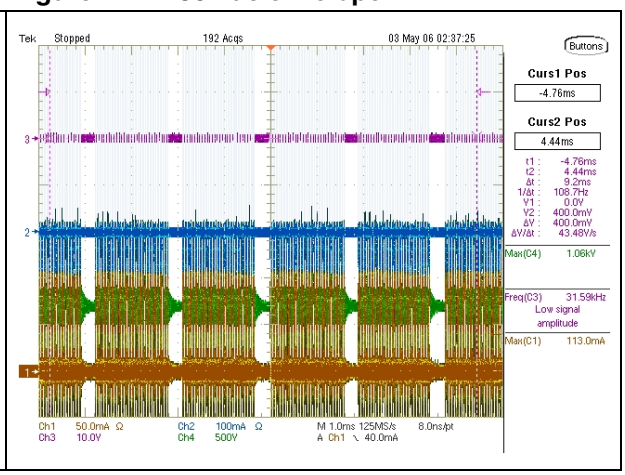


Figure 25. 600 Vac envelope

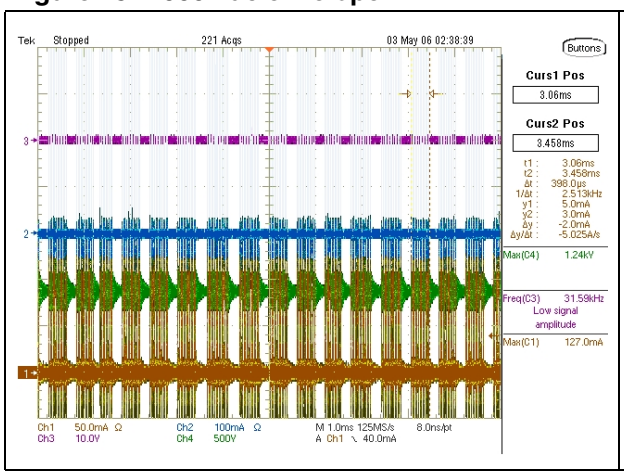
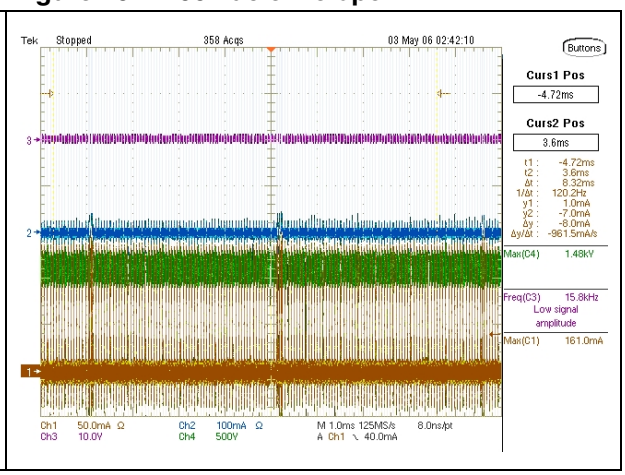


Figure 26. 760 Vac envelope



Appendix A Bill of material

Table 3. Bill of material

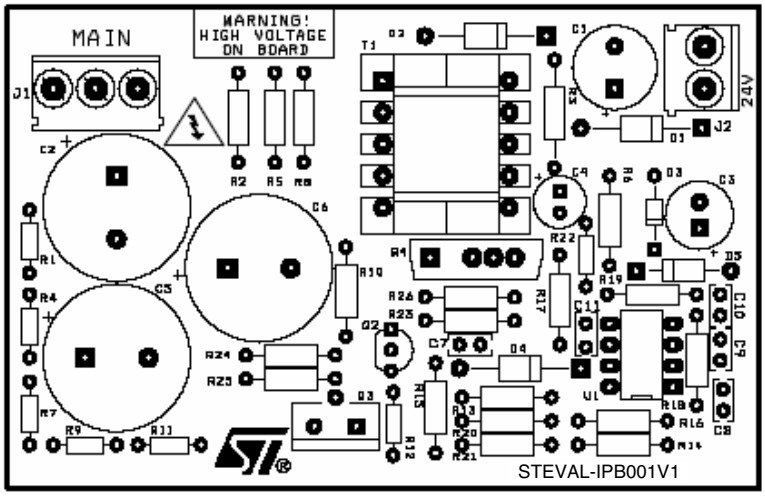
Reference	Quantity	Value/part number	Description
C1	1	ESF227M035AH2AA	Electrolytic capacitor, 220 µF/35 V, ARCOTRONICS
C2, C5, C6	3	ESZ336M450AM2AA	Electrolytic capacitor, 33 µF/450 V, ARCOTRONICS
C3	1	ESF337M025AH2AA	Electrolytic capacitor, 330 µF/25 V, ARCOTRONICS
C4	1	ESW476M025AC3AA	Electrolytic capacitor, 47 µF/25 V, ARCOTRONICS
C7	1	10 nF low voltage	Polyester capacitor, 50 V
C8	1	100 pF low voltage	Polyester capacitor, 50 V
C9	1	820 pF low voltage	Polyester capacitor, 50 V
C10	1	12 nF low voltage	Polyester capacitor, 50 V
C11	1	R82DC3100AA50M	Polyester capacitor, 100 nF/63 V, ARCOTRONICS
CON2	1	Bipolar connector	
CON3	1	Tripolar connector	
R1, R4, R7, R9, R11, R12	6	5.6 MΩ	Resistor, carbon film, 200 V, 0.125 W, 5 %
R2, R5, R8, R10, R24, R25	6	10 kΩ	Resistor, carbon film, 250 V, 0.25 W, 5 %
R3	1	1 Ω	Resistor, carbon film, 250 V, 0.25 W, 5 %
R6, R22	2	10 KΩ	Resistor, carbon film, 250 V, 0.25 W, 5 %
R13	1	680 kΩ	Resistor, carbon film, 250 V, 0.25 W, 5 %
R14	1	16 kΩ	Resistor, metal film, 250 V, 0.25 W, 1 % - for fine tuning
R15	1	3.3 kΩ	Resistor, carbon film, 250 V, 0.25 W, 5 %
R16	1	150 KΩ	Resistor, carbon film, 250 V, 0.25 W, 5 %
R17	1	22 Ω	Resistor, carbon film, 250 V, 0.25 W, 5 %
R18	1	2.2 kΩ	Resistor, carbon film, 250 V, 0.25 W, 5 %
R19	1	1 kΩ	Resistor, carbon film, 250 V, 0.25 W, 5 %
R20	1	100 kΩ	Resistor, metal film, 250 V, 0.25 W, 1 % - for fine tuning
R21	1	3.9 kΩ	Resistor, metal film, 250 V, 0.25 W, 1 % - for fine tuning
R23	1	6.8 Ω	Resistor, carbon film, 250 V, 0.25 W, 5 %

Table 3. Bill of material (continued)

Reference	Quantity	Value/part number	Description
R26	1	10 Ω	Resistor, carbon film, 250 V, 0.25 W, 5 %
D1, D2, D4	3	STTH110	Diode, high voltage ultra fast, 1000 V - 1 A, DO41, STMicroelectronics
D3	1	1N4148	Diode, 75 V, 0.15 A, DO-35
D5	1	20 V zener	Diode, zener, 20 V, 0.5 W
IC1	1	STUC3845B	Current mode PWM controller, Dip-8, STMicroelectronics
Q2	1	PN2222A	Small signal bipolar transistor, NPN, 40 V, 0.6 A, TO-92, STMicroelectronics
Q3	1	STP03D200	High voltage Darlington, NPN, 2 KV, 3 A, TO220, STMicroelectronics
Q4	1	STC04IE170HP	Emitter switched Bipolar transistor, 1.7 KV, 4 A, TO-247 4 L, STMicroelectronics
TR1	1	SRW20EF - E13H003	Transformer, TDK

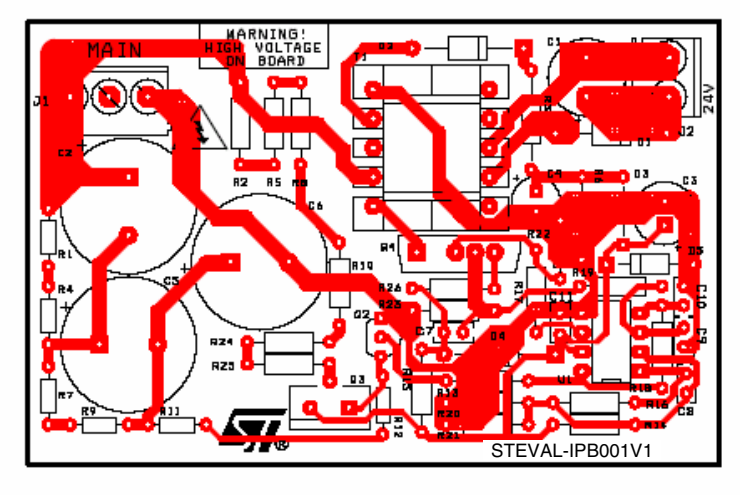
Appendix B Top view of the STEVAL-IPB001V1 demo board

Figure 27. Top view of the STEVAL-IPB001V1 demo board



Appendix C Bottom view of the STEVAL-IP001V1 demo board

Figure 28. Bottom view of the STEVAL-IPB001V1 demo board



10 Revision history

Table 4. Revision history

Date	Revision	Changes
19-Dec-2006	1	First issue